AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 11, as follows:

In accordance with the advancement of digital technologies, various digital signal processing technologies are proposed in wide fields. In the above-mentioned digital signal processing, an analog input signal is converted into a digital signal by an analog/digital (hereinafter, referred to as an A/D) converter and then is subjected to various signal processing by latter-stage circuits. A digital filter serving as a general digital signal processing circuit performs calculation for a plurality of sampling data which is continuously inputted, attenuates a frequency component other than a normal band from among frequency components included in sampling outputs, and extracts only desired frequency component data. In general, the digital filter uses a method for increasing the ~~number~~ amount of sampling data so as to improve an signal to noise (S/N) [[S/N]] ratio. However, ~~the increase~~ increasing [[in]] the ~~number~~ amount of sampling data causes [[the]] an increase in circuit scale and ~~the increase~~ in the amount ~~number~~ of calculation times[[,]] ~~and the prolongation of~~ thereby prolonging calculation time.

Please amend the paragraph beginning at page 2, line 1, as follows:

Generally, half-band processing is well-known to solve the problem. In [[the]] half-band processing, ~~an effect~~ the ability to reduce the number of elements is increased as the ~~number of~~ amount of sampling data is larger, and [[the]] calculation processing is facilitated by using the principle in that the S/N ratio of an output value is not changed upon setting a coefficient, which is multiplied by even-th sampling data, to be zero when the number of sampling data serving as a first processing target is odd. Since the coefficient is zero, the ~~number~~ amount of calculation times is half. As a consequence, the ~~numbers~~ number of

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~~multiplies~~ multipliers, adders, and complement control circuits and [[a]] the bit length of each register can be reduced.

Please amend the paragraph beginning at page 2, line 13, as follows:

However, since processing for the even-th sampling data is not performed in the half-band processing of the above-mentioned digital filter, it is equivalent that a sampling rate is reduced to [[be]] 1/2. Then, an aliasing-noise pass band [[upon]] when reducing the sampling rate is caused.

Please amend the paragraph beginning at page 2, line 18, as follows:

FIG. 1 is a diagram showing pass band characteristics of an output signal from the digital filter, in which the aliasing-noise is caused by the half-band processing, according to [[a]] background art. An aliasing band 1, occurring because of ~~occurred by~~ the half-band processing, occurs at almost ~~is caused near~~ a half frequency of a sampling frequency of the digital filter, as a pass band different from a normal band 2 serving as an original pass band. Therefore, the analog input signal includes a frequency component having the above band and, when the frequency component has an influence on signal processing at the ~~latter~~ later stage of the digital filter, the half-band processing cannot be used. Even ~~in the case of~~ when purposely using [[the]] half-band processing, a digital low-pass filter for anti-aliasing is necessary at the ~~latter~~ later stage of the digital filter. However, the digital low-pass filter needs calculation processing for a digital filter output and, therefore, the circuit scale and the number of calculation times are increased and the calculation time is long. An advantage for using the half-band processing to the digital filter is lost.

Please amend the paragraph beginning at page 3, line 19, as follows:

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To accomplish the above object, according to a first aspect of the present invention, there is provided a digital signal processing apparatus, comprising: [[1.]] A digital signal processing apparatus comprising: an A/D converter for converting an analog input signal into a digital signal; a digital filter for performing half-band processing to a sampling output of a digital signal outputted by the A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output; and an anti-aliasing circuit for suppressing or removing noise having an aliasing band, which is caused by the half-band processing in the digital filter, by using a sign signal outputted from the digital filter. Accordingly, a simple circuit structure can suppress the aliasing noise with low costs.

Please amend the paragraph beginning at page 5, line 17, as follows:

Advantageously, the anti-aliasing circuit may further comprise a delay circuit for delaying the output from the digital filter by a delay time which is taken by the measurement by the period measuring circuit and the comparison calculation by the comparator. Accordingly, the [[shit]] shift operation of the shift register, to which the delay data at the same time based on the output of the comparator, can be embodied with high accuracy.

Please amend the paragraph beginning at page 5, line 25, as follows:

Advantageously, the anti-aliasing circuit may comprise: a period measuring circuit for measuring a changing period of the sign signal which is outputted by the digital filter; a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band; a comparator for comparing and determining whether or not the period measured by the period measuring circuit is larger than the threshold set to the threshold holding circuit and for outputting a clear signal when it is determined that the period is not

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larger than the threshold; and a delay circuit for delaying the output from the digital filter by a delay time which is taken by the measurement of the period measuring circuit and the comparison calculation of the comparator and for erasing a signal during delay processing when the clear signal is inputted. Accordingly, the output of the unnecessary aliasing noise component can be prevented with [[the]] this simple structure.

Please amend the paragraph beginning at page 6, line 16, as follows:

According to a second aspect of the present invention, ~~there is provided~~ a digital signal processing apparatus ~~comprising~~ comprises: an A/D converter for converting an analog input signal into a digital signal; a digital filter for performing half-band processing to a sampling output of a digital signal outputted by the A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output; an edge-detection circuit for detecting an edge of a sign signal which is outputted by the digital filter and for generating a set pulse; a period measuring circuit for measuring a changing period of the sign signal which is outputted by the digital filter; a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band; a comparator for comparing and determining whether or not the period measured by the period measuring circuit is larger than the threshold held by the threshold holding circuit and for outputting a reset pulse when it is determined that the period is not larger than the threshold; and a detection register for inputting the set pulse so as to be in a set state and outputting a first level and for inputting the reset pulse so as to be in the reset state and outputting a second level. Accordingly, erroneous detection upon passage of the aliasing noise can be prevented.

Please amend the paragraph beginning at page 8, line 27, as follows:

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FIG. 2 is a block diagram showing a digital signal processing apparatus according to a second embodiment of the present invention. Referring to FIG. 2, the digital signal processing apparatus comprises: an A/D converter 3 for converting an analog input signal 10 into a digital signal; a digital filter 4; and an anti-aliasing circuit 6 provided at the ~~latter~~ later stage of the digital filter 4, for suppressing aliasing noise by using a sign signal 5 outputted from the digital filter 4. The anti-aliasing circuit 6 determines whether the signal from the digital filter 4 is a signal having a normal band or the aliasing noise, by using a changing period of the sign signal 5, and attenuates only an aliasing noise component of the output from the digital filter 4. Consequently, although the half-band processing has not been used for the digital filter under the limitation of the number of mounted elements, it can be used for the digital filter. The digital filter purposely using the half-band processing does not need the low-pass filter which is arranged at the ~~latter~~ later stage of the digital filter. For example, when both the sampling data and the ~~coefficient~~ coefficients are 10 bits, several ~~thousands of~~ thousand elements are necessary for each multiplier. On the other hand, the anti-aliasing circuit 6 comprises approximately one thousand elements. Therefore, ~~an effect in that~~ several ~~thousands~~ thousand to several tens of thousands of elements can be reduced ~~can be obtained~~ without using the low-pass filter.

Please amend the paragraph beginning at page 9, line 27, as follows:

FIG. 3 is a block diagram specifically showing one example of the anti-aliasing circuit in the digital signal processing apparatus. The digital signal processing apparatus comprises the A/D converter 3, the digital filter 4, and the anti-aliasing circuit 6. An analog input signal 10 is converted into a digital data signal D1 by the A/D converter 3. A frequency component within a preventing area, included in the digital data signal D1, is attenuated by the digital filter

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4 which is subjected to the half-band processing. However, [[the]] aliasing noise~~, which is~~ caused by [[the]] half-band processing[[,]] is mixed in an output signal D2 from the digital filter 4. The output signal D2 of the digital filter 4 is inputted to the anti-aliasing circuit 6.

Please amend the paragraph beginning at page 13, line 10, as follows:

Referring back to FIG. 4, the sign changing period of the sign signal 5 is measured based on the output signal D2 after the half-band processing (step S7). The measured sign changing period of the sign signal 5 is compared with a threshold [[A]] (step S8). The threshold [[A]] is set in advance to establish a relationship of (sign changing period (M) < threshold (A) < sign changing period (N)). If the comparison result, when the sign changing period M is smaller than the threshold A, is "1", the shift control signal 16, serving as the comparison result, becomes "1" only during the occurrence of the aliasing noise, as shown by [[a]] waveform 24. Therefore, the shift control signal 16 can be used as a detection signal of the aliasing band pass signal. Incidentally, the waveform 24 is delayed from the waveform 19 by a delay time Td. Thus, the output signal D2 of the digital filter 4 shown by the waveform 19 is subjected to [[the]] delay processing by the delay time Td by the delay circuit 15. Then, [[the]] output signal D2 is stored in the shift register 13 as the signal D3 shown by an amplitude image waveform 25. The signal shown by the waveform 24 is obtained as the comparison result and is inputted to the shift register 13 as the shift control signal 16.

Please amend the paragraph beginning at page 14, line 5, as follows:

If the sign changing period M is smaller than the threshold A, that is, if the waveform 24 is "1", the shift register 13 assumes that [[the]] aliasing noise is input[[ted]] and then shifts the output from the digital filter 4, which is stored in the shift register 13, at the same time, ~~which is stored in the shift register 13,~~ in the LSB direction by one bit (step S9), and suppresses

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the amplitude to [[be]] a half. On the other hand, if the sign changing period is larger than the threshold A, ~~that is~~ i.e., if the waveform 24 is "0", the shift register 13 assumes that the normal-band signal is input[[ted]], and a signal indicating that the shift operation is not performed is output[[ted]] (step S10). The signal is output[[ted]] without the shift processing of the shift register 13 (steps S5 and S6). In this case, a waveform 26 represents an amplitude image of an output signal 17 of the shift register 13. As described above, the amplitude of only the aliasing noise can be suppressed without changing the amplitude of the normal-band signal.

Please amend the paragraph beginning at page 14, line 23, as follows:

FIG. 6 is a diagram showing another example of the anti-aliasing circuit according to the first embodiment of the present invention. In the anti-aliasing circuit shown in FIG. 6, a shift value setting register 27 for controlling the number of bits of the shift register 13 is [[newly]] added. Consequently, the amount of attenuation of the output data from the digital filter 4 can arbitrarily be adjusted when the aliasing noise is detected. Namely, when a number n of bits of the shift register 13 is set to the shift value setting register 27, an amplitude of the output data is 1/(2n).

Please amend the paragraph beginning at page 15, line 7, as follows:

FIG. 7 is a diagram showing further another example of the anti-aliasing circuit according to the first embodiment of the present invention. Herein, the shift register 13 shown in Fig. 2 is deleted and the output of the comparator 12 is set to be a clear signal 29 of the delay circuit 28. The delay circuit 28 delays the output from the digital filter 4 by a delay time which is taken by the measurement of the period measuring circuit 14 and by the comparison calculation of the comparator 12, and erases a signal during the delay processing when the clear

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signal 29 is input[[ted]]. With the above-mentioned structure, the unnecessary aliasing noise component can completely be removed.

Please amend the paragraph beginning at page 15, line 20, as follows:

FIG. 8 is a block diagram of a detection device using a sign signal of the output from the digital filter according to a second embodiment of the present invention, and FIG. 9 is a timing chart of signals from block units in FIG. 8. In a detection device 7 shown in FIG. 8, the period measuring circuit 14 measures a sign changing period of a sign signal 34 from the digital filter 4, and the comparator 12 compares the measured sign changing period with the threshold which is set to the threshold holding circuit 11. If the sign changing period measured by the period measuring circuit 14 is smaller than the threshold, it is determined that the aliasing noise is detected and a reset pulse 35 is generated. A waveform 39 shown in FIG. 9 represents an amplitude image of an output 33 from the digital filter 4. The sign signal 34 from digital filter 4 is input[[ted]] to an edge-detection circuit 30, a rise edge is detected, and a set pulse 36 is generated to a detection register 31. By adding the reset pulse 35 to a reset terminal of the detection register 31, an output signal 38 of the detection register 31 is set to be "0" during detection of the aliasing noise and erroneous detection due to the aliasing noise is prevented. Incidentally, if the set pulse 36 is not input[[ted]] to the detection register 31 during a period (T + ΔT) which is longer than a sign changing period T of the output 33 from the digital filter 4, a state-detection circuit 32 outputs the reset pulse 35 to the detection register 31.

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